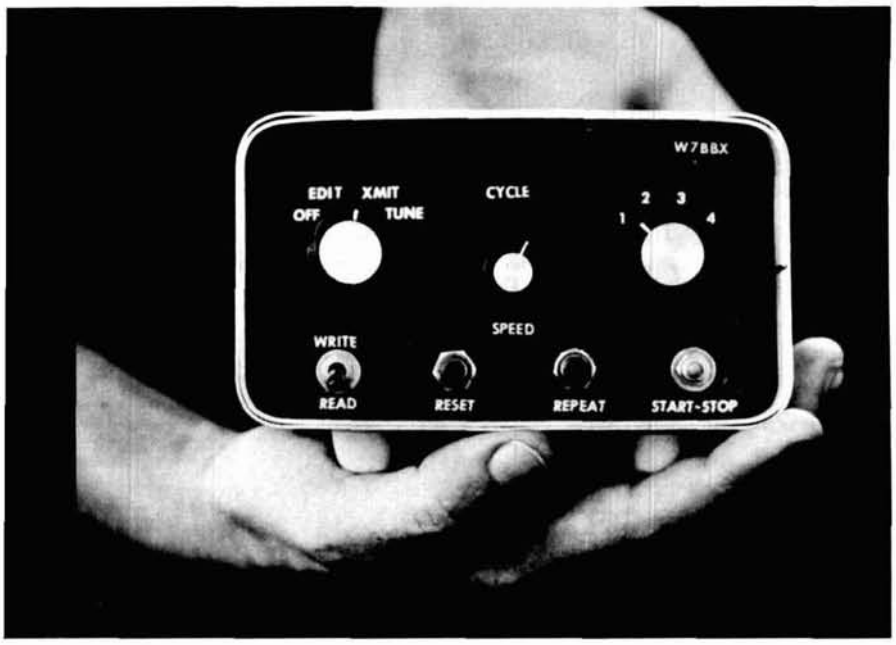

programmable contest keyer

A CW man's keyer featuring high memory capacity, operating convenience, and reasonable cost

A programmable memory keyer is a desirable asset in contest work. It can handle much of the repetitive work while you check dupes, fill out the log, or just take a break. The few programmable keyers on the market all have some desirable features, but they lack the capacity and automatic memory control necessary for smooth, high-speed contest operating. A programmable memory keyer is also needed that the average amateur can afford. The keyer described here has been designed to meet these needs.

Major design objectives included high memory capacity, low cost, and operating simplicity for both program and readout modes; manual, semiautomatic, or fully automatic operation; nonvolatile, nondestructive memory readout; and convenient size. The design is centered around the Intel P2102, a 1024-bit static programmable random access memory (PRAM) in a 16-pin package.* This IC was selected because it requires no refresh circuitry as do dynamic PRAMS, only a single +5 volt power supply is required, all inputs and outputs are fully TTL compatible, and it's readily available at reasonable cost.

description

The keyer (**fig. 1**) is designed so that manual operation with a paddle or bug will always override the mem-

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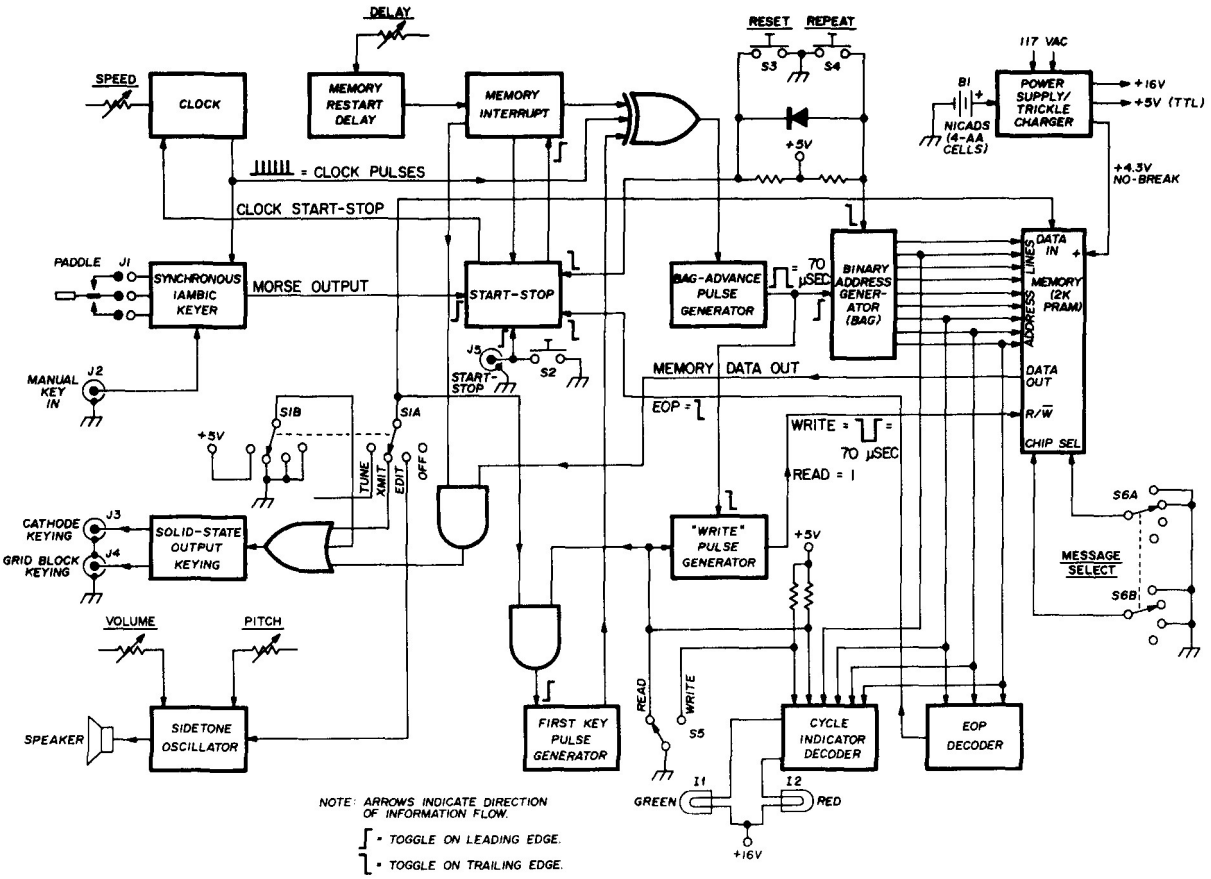


fig. 1. Simplified block diagram of the programmable contest keyer designedby W7BBX. Features include iambic keying, four selectable 512-bit memories, built-in sidetone oscillator, and solid-state transmitter keying.

ory readout. Operation is identical to that of a conventional digital iambic keyer when the memory section isn't used. The popular clock and iambic keyer described by Garrett[1] were modified slightly to interface with the memory. The synchronous clock begins at the instant the paddle is closed and runs for two clock pulses after character generation ceases. The self-completing characters are perfectly formed and spaced throughout the speed range, and character generation is jam-proof. Speed is continuously and smoothly variable from about 8 wpm to well above 60 wpm. The dot memory allows automatic insertion of a dot while holding the dash paddle closed. Similarly, a dash may be inserted while holding the dot paddle closed. Iambic operation allows alternate perfectly spaced dots and dashes to be generated when both paddle arms are simultaneously closed. An external manual key or bug can be used directly instead of the paddle and will control all keyer and memory readout functions.

Solid-state output keying for all inputs (paddle, external manual key and memory readout) is incorporated. The keyed output is directly compatible with most popular cathode-keyed and sidetone/vox actuated and grid-block-keyed transmitters; two output keying jacks, one for positive-keyed voltages up to +150 volts and one for negative-keyed voltages up to -150 volts, are simultaneously available on the rear panel. However, if your transmitter is cathode keyed and 100 mA or more flows through the keyed circuit, an external pass transistor or keying relay may be required. A twin-T audio oscillator and amplifier provide a sinusoidal sidetone waveform that drives an internal 8-ohm permanent-magnet speaker with sufficient audio to perform well in a moderate ambient noise environment. Volume is adjustable, and the pitch is variable from about 400 to 1500 Hz. The internal sidetone oscillator is activated only during the edit mode; that is, for off-the-air programming or checkout of a programmed message. During transmit, or while programming on the air, the transmitter sidetone oscillator would be used in the usual manner. If your transmitter doesn't have an internal sidetone oscillator, a minor wiring modification to the function switch S1A terminals will permit the keyer's internal sidetone oscillator to be used in both edit and transmit modes. A *tune* position is incorporated for tune-up purposes.

memory readout

With S5 in *readout* (**fig. 1**) and the stored message to be transmitted selected by S6, readout is initiated by depressing S2. This starts the clock, and the clock pulses are fed to the binary address generator (BAG), which includes nine tandem flip-flops. As the flip-flops cycle

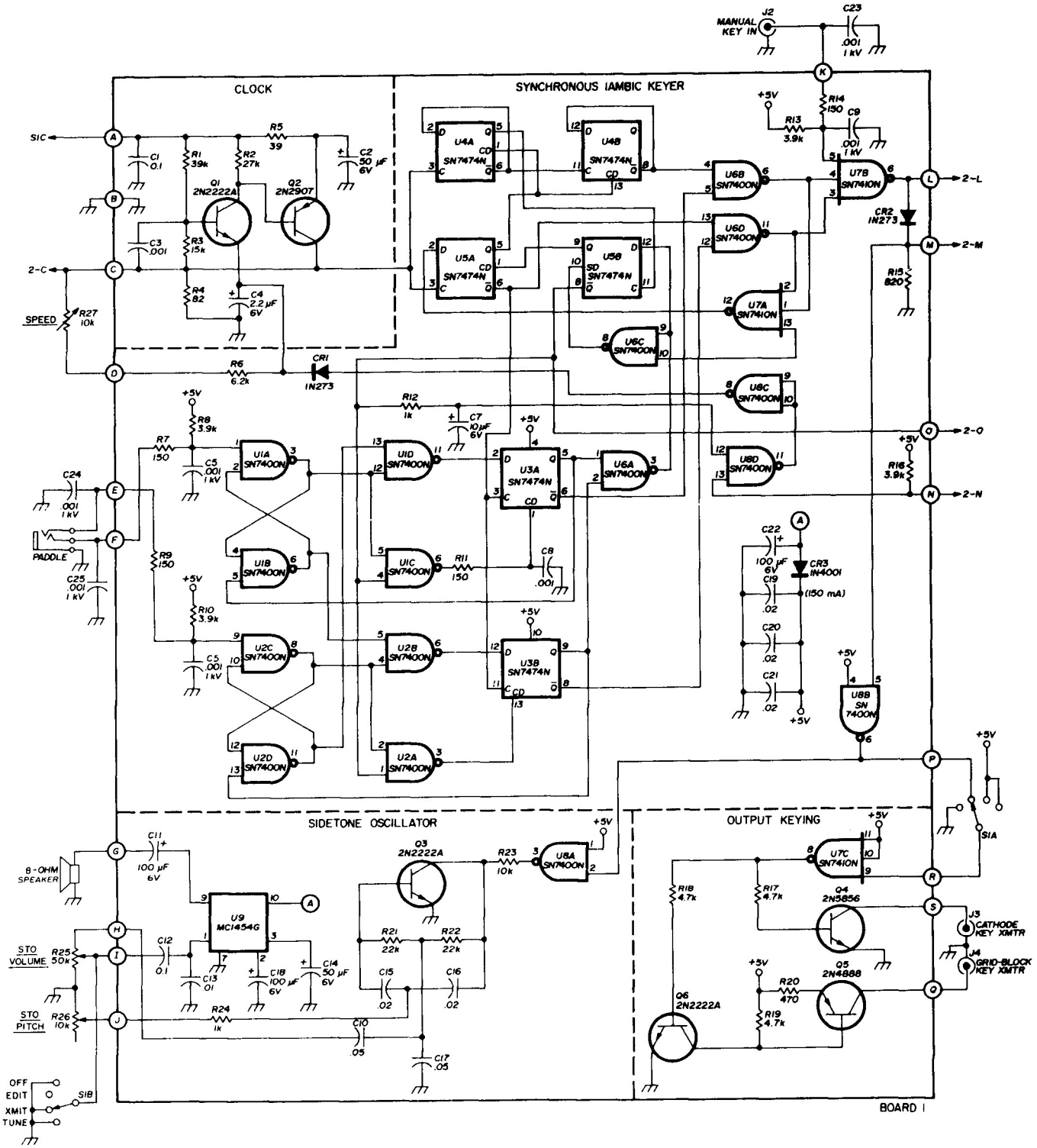


fig. 2. Logic diagram of the keyer board for the programmable contest keyer. Designations 2-C, 2-L, etc., indicate connections to board 2 (fig. 3). S1 is a 3-pole, 4-throw shorting-type rotary switch. All resistors are ¼ watt, 10%.

through 511 successive counts, their BCD output is applied to the nine address lines of the selected memory section, and the addressed information stored in each memory cell is automatically presented to the memory chip data out terminal. If desired, memory readout can be halted in mid message by depressing S2 again before completion of the entire readout sequence. Further memory readout is inhibited until S2 is again depressed;

memory readout will then continue from the point at which it was interrupted (semiautomatic operation). On the 511th clock pulse fed to the binary address generator, the BAG returns to all zeroes on the nine output lines (end of program readout). The downward transition of the highest significant memory address line is unique and signifies "end of program," or EOP. This EOP transition automatically stops the clock, and all control circuitry is simultaneously reset to begin another readout sequence when S2 is next depressed.

Rear-panel provisions are made for remotely starting the memory readout sequence. A separate spst switch in parallel with S2 at J5 can control both *start* and *stop* functions; for example, a simple foot switch can be used to free your hands for the paddle or logging. Alternatively, any external circuit that provides a negative-going TTL-compatible pulse can trigger *readout*. (One possible application might be synchronization to WWV for moonbounce, meteor scatter, or satellite relay operations.)

When the memory readout cycle is initiated, the green *cycle* indicator (I1) lights continuously until 87.5% of the memory contents have been read out; at which point it begins to flash to indicate "nearing end of program." When the message has been completely read out, the green light extinguishes. Depressing S3 at any point in the message *readout* cycle stops the clock and resets all control functions and the binary address generator. Depressing S4 during the first seven-eighths of the message readout sequence resets only the binary address generator to the message beginning, which is then automatically repeated. Thus, if "CQ TEST DE W7BBX/4" were programmed into the memory, selective repeats by S4 can modify the transmitted message to, for example, "CQ CQ TEST CQ TEST DE W7BBX/4." The increased memory capacity over that of many presently available keyers allows a message length up to that of "The quick brown fox jumped over the lazy dogs back" to be programmed into each of the four separate memories.

Controls and receptacles on rear panel. Although not labelled, one jack is for grid-block keying; the jack labelled "to xmtr key" is for cathode-keyed transmitters.

An essential feature of a contest keyer is the ability of the paddle to override the memory readout to insert exchange number and/or signal reports in the middle of a programmed message (fully automatic operation). The memory interrupt feature allows you to manually break into any point of the memory readout cycle merely by activating either the paddle or external manual key during memory readout; memory readout is instantly interrupted and remains interrupted as long as manual keying continues. When manual keying stops, an adjustable 1-second delay is introduced by the memory restart delay before the keyer automatically allows memory readout to continue from the point at which it had been interrupted. Memory restart does not have to be manually commanded. Thus, a programmed contest message of "DE W7BBX/4 NR 599 VA BK" can be sent correctly by manually inserting the contest exchange number be-

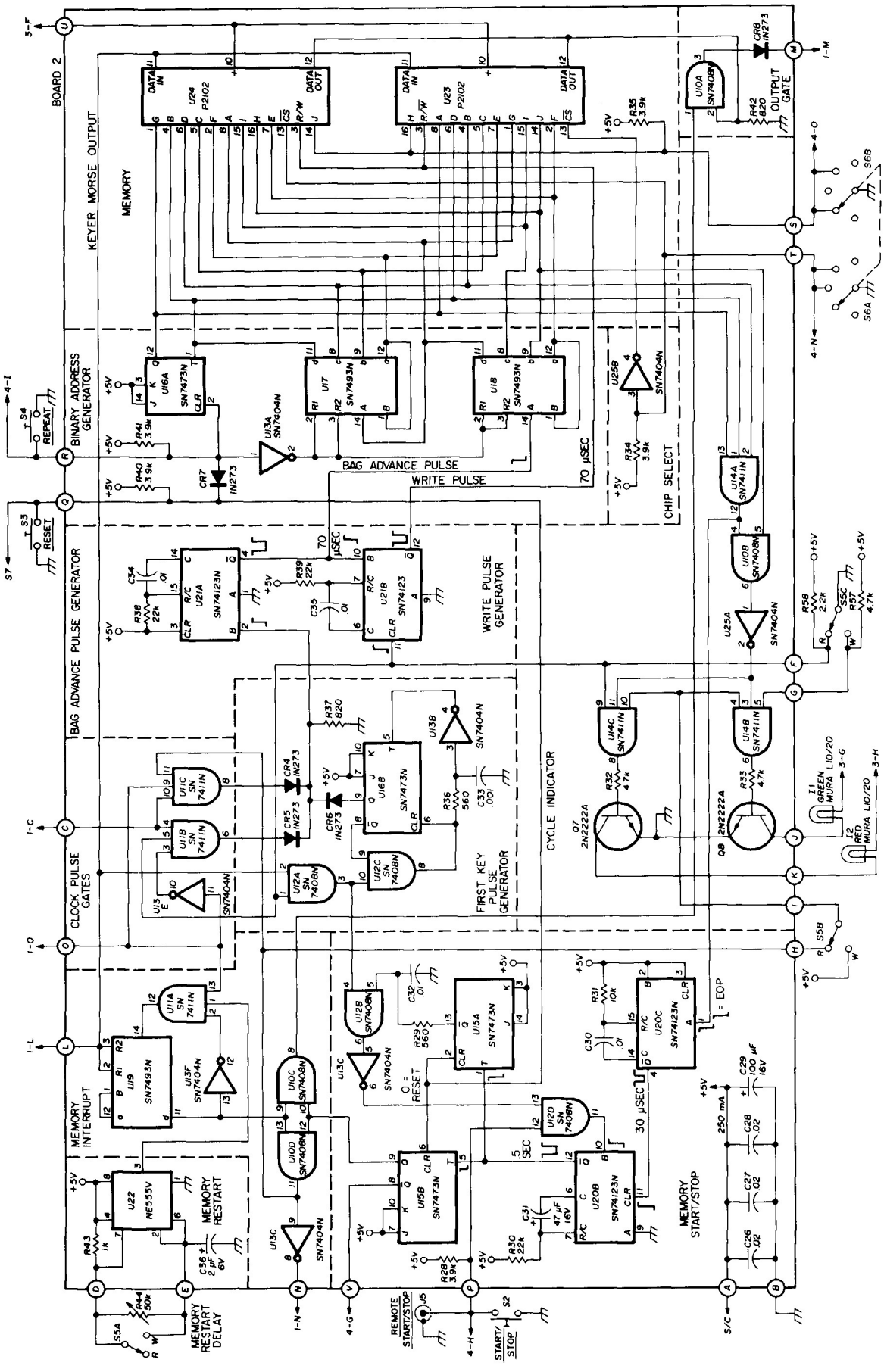


fig. 3. Memory circuit for the programmable contest keyer. Designations 1-L, 1-O, etc., designate connections to board 1 (fig. 2.) Connections 3-F, 3-G go to the power supply, and 4-N, 4-O go to the remote control unit. S2, S3 and S4 are spst push buttons. S5 is a 3pdt toggle switch; S6 is a 2-pole, 5-throw rotary switch (shorting or non-shorting okay). All resistors are ¼ watt, 10%.

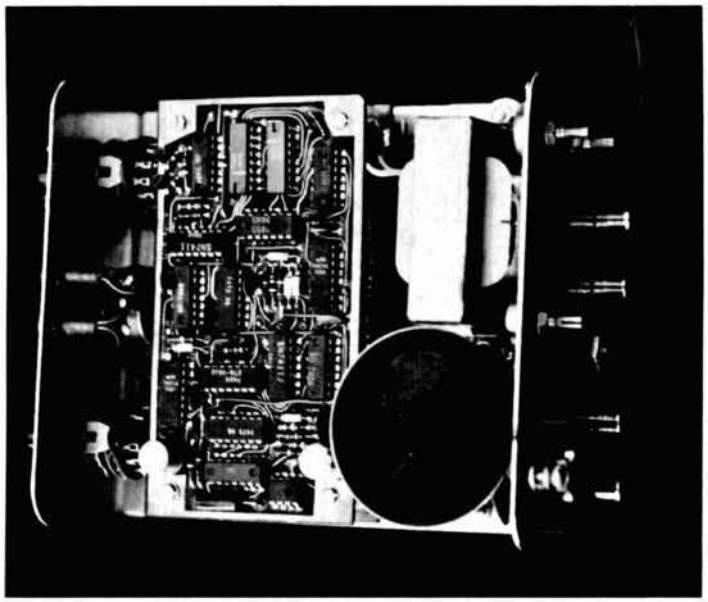
tween NR and 599 during memory readout. Memory contents previously stored in the array are automatically prevented from being inadvertently transmitted while the memory is in a hold condition during manual keying.

memory programming

Placing S5 in the *write* position automatically programs a logic zero in the first cell, steps the binary address generator to the second cell, and causes the red *cycle* indicator (I2) to light immediately, even though the clock is not yet running and nothing is being written into the memory register. The clock is started and programming begins automatically merely by activating the paddle. During the *write* sequence, the clock operates in a "semi-synchronous" mode: while keying normally with the paddle, operation is fully synchronous; if character generation ceases, the clock continues to run asynchronously through the remainder of the message capacity, and logic zeroes are programmed to erase any previously stored message.

The red *cycle* indicator begins blinking when 87.5% of the memory has been programmed and returns to steady red at the end of the programmable capacity; this reminds you to place S5 to the *read* position before initiating a *readout* sequence with S2, or again activating the paddle before a new memory register is selected by S6. Otherwise, the message contents just programmed might be erased.

With S5 in the *write* position, the *write* pulse generator is activated. The binary address generator "advance" pulses toggle the BAG on the leading edge of each positive-going pulse, while each trailing (falling) edge triggers the *write* pulse generator to provide the negative-going *write* command to the memory array. Thus, correct timing occurs for accurate memory cell selection and for writing into the selected cell the logic level that appears on the data-in line (keyer output) at the instant of the *write* pulse. S1 and S5 are independent, so the keyer may be programmed on the air (S1 in *transmit* mode) or off the air (S1 in *edit* mode).



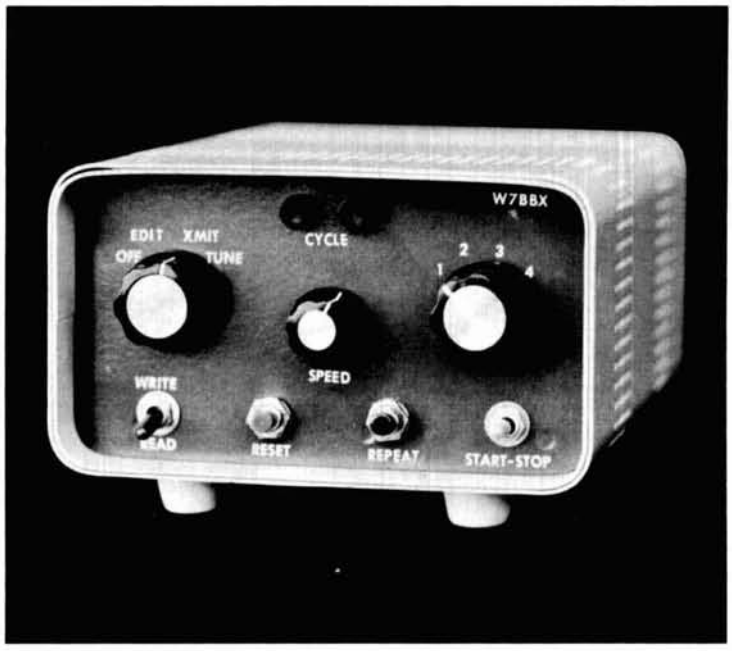
Chassis top view showing memory board, sidetone oscillator speaker, and power supply transformer.

power supply

Although the Intel P2102 has nondestructive memory readout (stored information is not lost during readout), loss of power to the memory chip causes loss of the entire stored information (the memory chip is volatile). To keep Murphy and his despicable laws out of the memory, a no-break trickle-charged nicad supply is recommended. Such a charger will preserve keyer memory contents for about 2 to 3 hours, which will eliminate reprogramming when your Field-Day generator runs out of gas. Completely discharged nicads will be recharged in about 20 hours.

remote operating control

Provisions can be made on the rear panel of the contest keyer to accommodate a remote operating control which can be conveniently placed next to your paddle or bug.* The remote unit controls those keyer readout functions which are most necessary during a contest: message selection, message start, message repeat, and message reset. Depressing any one of the four message select pushbuttons antomatically selects that message, resets the memory to the message beginning and starts meassage readout. Since message selection is



Front panel of programmable contest keyer. Set and forget controls, and input and output jacks, are on rear panel.

*Schematic diagrams for the power supply and remote-control unit will be sent to interested readers upon receipt of a stamped, self-addressed envelope.

independent of the last message sent, successive selections of the same message immediately repeats that message from its beginning. A separate *reset* pushbutton is included to immediately stop the readout sequence.

Remote control unit for the programmable contest keyer provides control of all major keyer functions.

The remote cabinet selected (LMB CR-531) is approximately 1x3x5 inches (2.5x7.5x1.3cm) and houses the five pushbuttons, the printed-circuit board and four optional panel lights which indicate the selected message. Connection to the keyer is made by a plug-in, shielded, 8-conductor cable. All power for the remote is derived from the keyer, and removal pf the remote cable from the keyer does not affect keyer operation.

construction

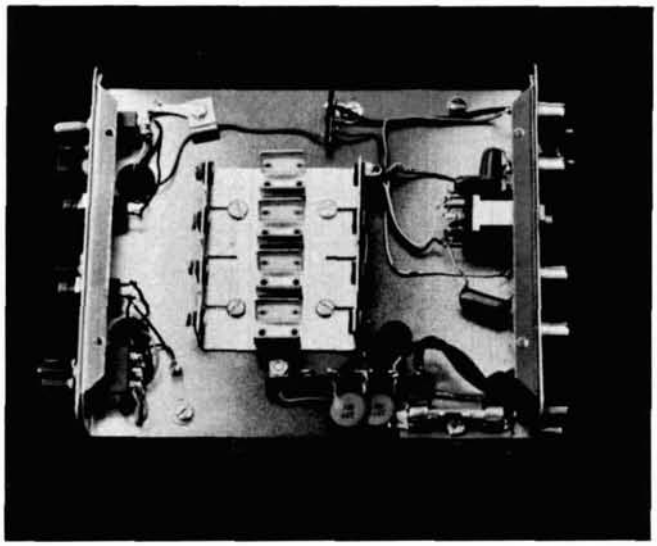
Panel clutter was avoided by automating as many memory-control functions as possible. Most-used controls are on the front panel; others are mounted on the rear of the keyer. An LMB CO-3 enclosure was used. The circuit is mounted on three PC boards: one for the basic iambic keyer, output keying, and sidetone oscillator; one for all memory functions; and one for the power supply.†

If desired, the keyer may be built without the memory board and used as a conventional iambic keyer and the memory may be added later. No keyer-board changes will be required and only four wires need be interconnected between keyer and memory board. The PC-board layout allows all memory-board wires and connections to be added without removing either keyer board or power supply from the cabinet.

A high degree of rf immunity is achieved by a) using TTL instead of CMOS devices, b) providing rf bypassing on all paddle and keying leads, and c) providing a grounding bond between cabinet sections. The keyer has been successfully kilowatt tested at a 3:1 vswr from 80 through 10 meters.

summary

The trade between performance, cost and circuit simplicity is sometimes difficult. For this project it was decided to opt for a capacity of four 512-bit messages and gain the advantages of paddle-programming and fully-synchronous operation at the expense of increased circuit complexity. This decision has been proved by the keyer's flexible, reliable, and unconfusing operation. This keyer has been a most useful operating aid both at home and in the field under generator power (thanks to the nicads). I'd like to thank the members of the Potomac Valley Radio Club for their constructive comments, suggestions and support.



Underchassis view showing battery receptacles and power-supply wiring.

†A set of double-sided PC boards with plated-through holes plus assembly and operating instructions are available from HFB Enterprises, Post Office Box 667, Herndon, Virginia 22020. The price is $30.00 post paid. Included are step-by-step assembly instructions, a complete parts list, operating instructions, and a full set of drill templates for the LMB CO-3 and LMB CR-531 cabinets.

reference

1. James Garrett, WB4VVF, "The WB4VVF Accu-Keyer," *QST*, August, 1973, page 19.

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