cosmos IC electronic keyer

Applying cosmos technology to a versatile, compact, low-drain keyer design

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Since the advent of ICs on the amateur radio scene, a number of articles on keyers have appeared in the amateur magazines. Now that c-mos or cosmos ICs have become available to the amateur from various sources at modest prices,* it's time that these "state of the art" building blocks found an application in a homebrew project.

The cosmos keyer described here draws only 0.4 mA on standby, with an average key-down current drain under 2 mA at a supply voltage of 10 volts. The keyer can work properly with supply voltages from 4 to 15 volts. When operated at 5 volts, the keyer actually consumes less than 100 microamps, less power than a set of headphones! Its low power requirement makes it ideal for the QRP or field day enthusiast. If TTL logic was substituted for the cosmos ICs in this keyer, the current drain would be in excess of 200 mA.

Some of the more important features of an electronic keyer using cosmos ICs is low power consumption, simple construction and modest construction cost (about $10.00 for parts). The keyer described in this article features self-completing dots, dashes and spaces, a built-in transmitter keying circuit and sidetone generator and small size – the circuit board can be mounted inside your favorite rig.

*Poly Paks, Inc., Box 942, South Lynnfield, Massachusetts 01940.

The basic clock gating circuit used in the keyer is illustrated in **fig. 1**. The clock gate allows only full clock pulses to pass through it, regardless of the timing inaccuracies of the *enable* signal. No partial pulses or "slivers" can be tolerated if a keyer is to send perfect code.

In **fig. 1**, U1 is a type-D flip-flop. The logic level present at the *data* or D input will be transfered to output Q at the next positive going edge at the *clock* input (pin C). Notice that the clock feeds pin 1 of U2, pin 1 of U3 and pin C of U1. U2 is the output gate and U3 is the reset gate.

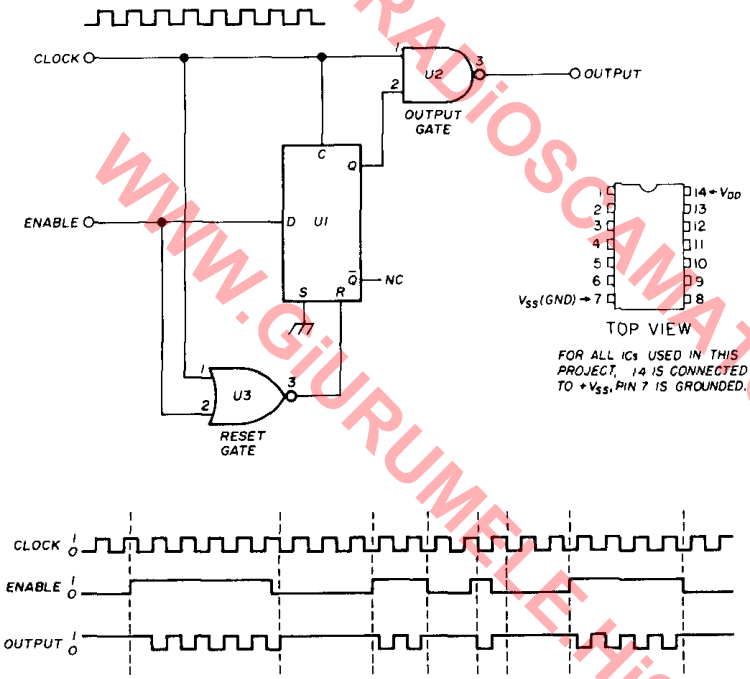


fig. 1. Basic clock gating circuit for the cosmos keyer.

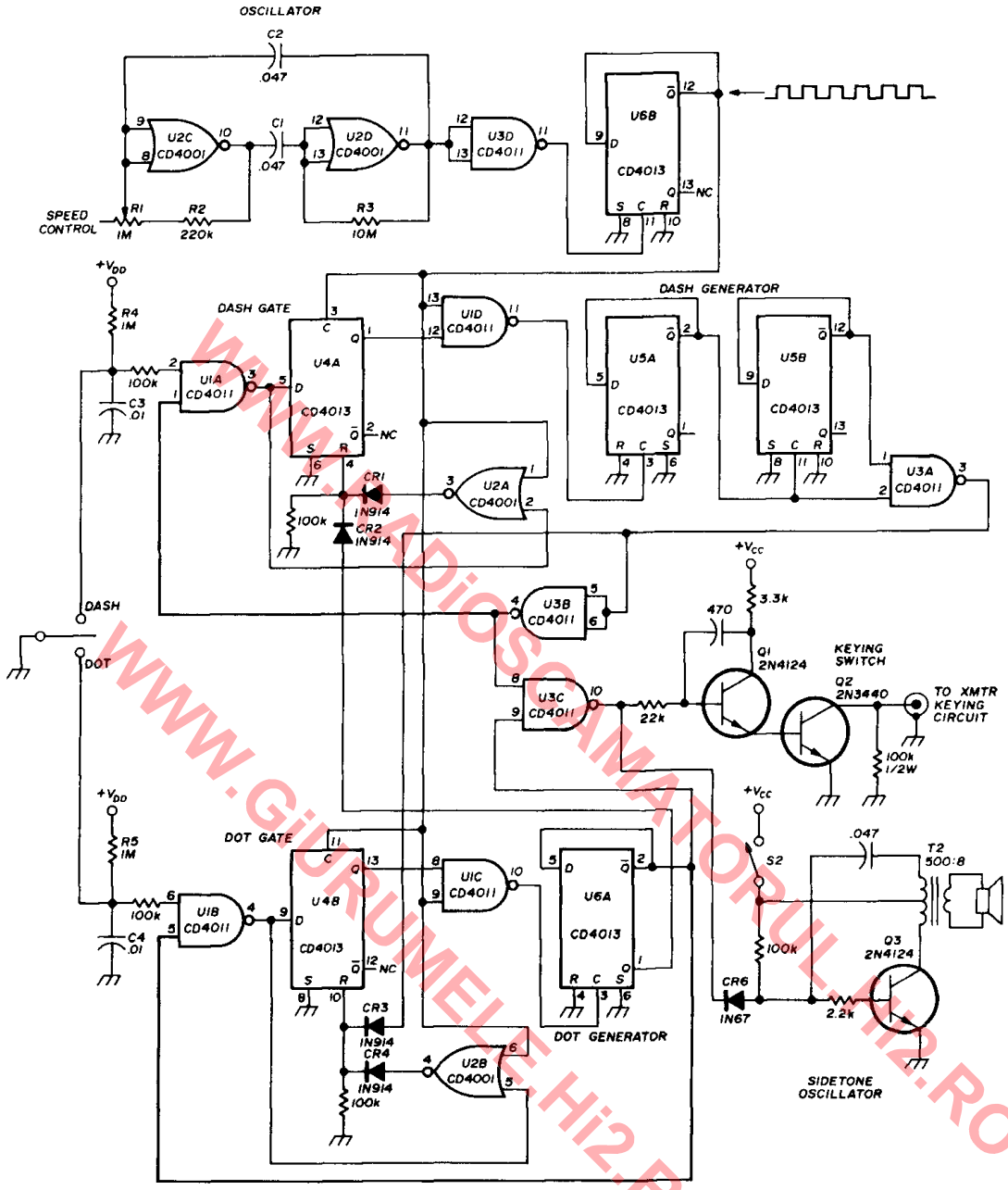
When the *enable* signal is low (zero), pin Q of U1 is assumed to be zero if pin C is being clocked. As long as pin Q of U1 is zero, U2 will not pass the clock pulses. Also, as pin D of U1 is zero, the clock pulses at pin 1 of U3 will pulse the reset pin (pin R) of U1. A 1 on the reset pin of a cosmos flip-flop will force Q to zero and will override all other input signals. The *set* pin of U1 is grounded for this reason. A 1 at the *set* pin will force Q to a 1 and will override all other input signals.

When the *enable* signal goes to a 1, pin Q will go to a 1 at the next positive-going clock pulse leading edge. Now that pins 1 and 2 of U2 are 1, pin 3 goes to zero and will go to a 1 when the negative-going clock transition occurs. Thus the output of U2 is the inverted version of the clock pulses.

When the *enable* goes to zero, flip-flop U1 will be reset by the NOR gate U3 at the time when the clock is zero. If the NOR gate were not used to reset U1, then the next positive-going edge of the clock pulse would appear at the pin 1 of U1 simultaneously with the negative transition at pin 2 of U2 due to the data transfer action of flip-flop U1. Thus you would have logic levels changing simultaneously in opposite directions at pins 1 and 2 of U2. This would result in a "sliver pulse" at pin 3 of U2 when the input signals cross the threshold level of U2. To prevent this from happening, the reset gate U3 is used to reset the flip-flop when both the *enable* and *clock* inputs are at zero.

final circuit

The circuit I finally settled on for my cosmos keyer is shown in **fig. 2**. The keyer generates dashes and dots at a fixed time ratio of 3 to 1. A space has the same duration as a dot. The time base of the keyer is generated by two NOR gates, U2C and U2D, connected in a class-A multivibrator configuration. Resistor R3 causes U2D to self bias into a class-A condition, with the output reaching a dc level equal to the threshold of the gate itself (about 45 percent of the supply voltage). Resistors R1 and R2 have the same effect on U2C. The time constant (R3-C1) is much greater than (R1 + R2)C2 so the frequency of the oscillator

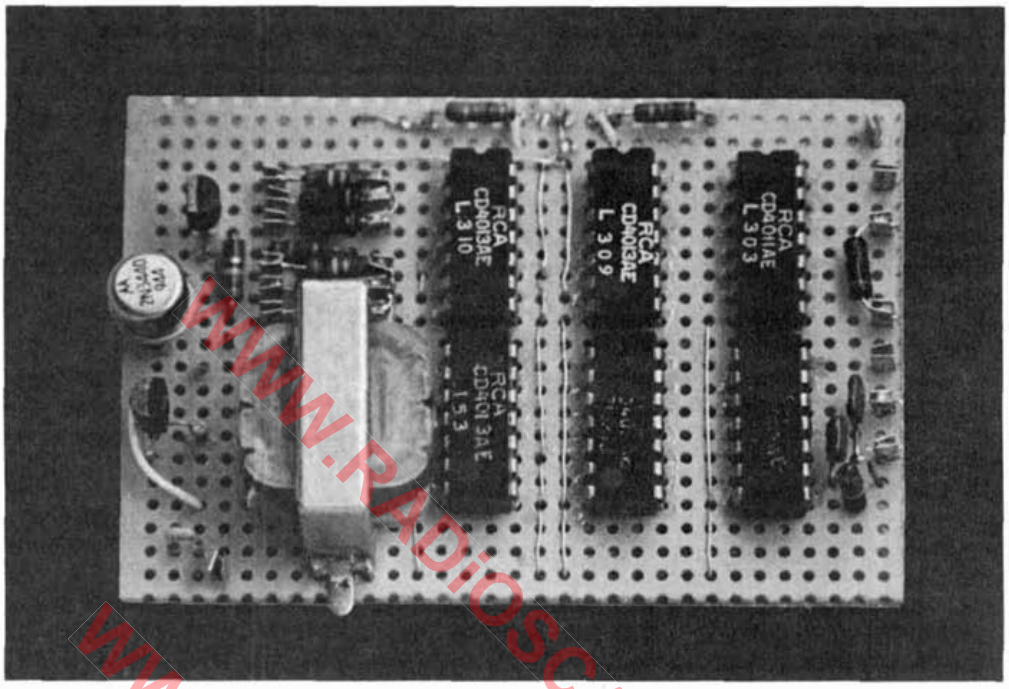


R1	1 megohm linear taper potentiometer	U2	cosmos NOR gate (CD4001 or equivalent
T2	500 ohm CT to 8 ohm transformer (Radio Shack 273-1381)		
U1, U3	cosmos NAND gate (CD4011 or equivalent)	U4, U5 U6	cosmos dual D flip-flop (CD4013 or equivalent)

fig. 2. Complete schematic diagram for the cosmos keyer. The bold lines are the feedback paths for the dot and dash generators, which allow them to end their timing in sync with the clock after paddle release. The sidetone generator, lower right, is optional.

is inversely linear with the setting of R1. Inverter U3D buffers the oscillator and squares up its output. Flip-flop U6B divides the oscillator frequency by two, but more importantly, provides a clock source with a perfect 50 percent duty cycle.

Note that the dot and dash generators each have their own clock gates, and are connected in such a manner that which-



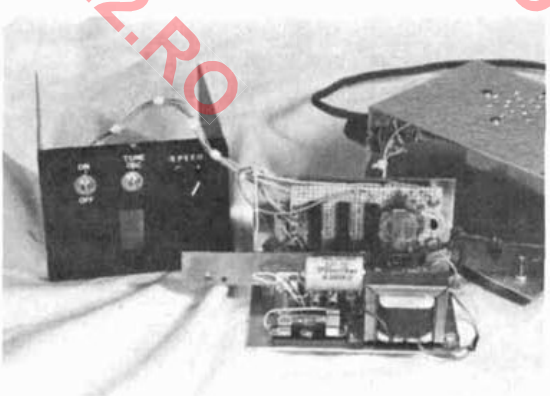
Logic circuitry for the cosmos keyer is wired on small section of perforated circuit board. Keying transistor and sidetone circuit are to the left.

ever of the two gates is enabled first overrides the other until its timing cycle is completed. If the dot gate is enabled first, the dash gate will be held in reset via diode CR2 until the timing cycle for the dot is completed, even if the dash paddle was depressed. Also, a complete space period would elapse before a dash could be sent, and vice versa. Diode CR3 allows the dash gate to reset and override the dot gate while dashes are being sent. The RC networks R4-C3 and R5-C4 provide pull-up bias for gates U1A and U1B and also eliminate the effect of key contact bounce.

The dash generator consists of a four-state binary counter (U5A and U5B) and a gate (U3A) to decode the four count states into dashes that are three clock periods long, separated by spaces one clock period long. U3B inverts the output of U3A to provide the proper logic levels to U3C by cancelling the inverting effect of U3A.

The bold lines are the feedback paths for the dot and dash generators. These feedback lines allow the dot and dash generators to end their timing in synchronization with the clock after their respective paddles have been released. This is what adds the self-completing feature to the keyer.

The output gate U3C drives the Darlington pair Q1 and Q2. Transistor Q2 is a high-voltage device, the Motorola 2N3440, which has a 250-volt B_{vcb} rating. If you plan to use the keyer solely



Construction of the cosmos keyer. Circuit board, keying mechanism and power supply are on center chassis. Speed control and switches are mounted on front panel, left.

for your solid-state QRP rig, then just about any 5-watt npn transistor will do the job.

The largest portion of the standby current drain can be attributed to the oscillator. When the threshold region of a cosmos device is entered at a slow rate (such as by RC decay), the device draws relatively large amounts of current. The increase in current during key-down conditions is caused by the conduction of Q1 in driving Q2.

important

When working with cosmos ICs it's important to remember to *never* leave unused input pins floating. *Always* make sure that any unused input pin is tied to either ground or to V_{dd}, whichever is logically appropriate. For example, the *set* and *reset* pins of U5 and U6 have been tied to ground. If this precaution is not observed, these high impedance inputs are wide open for electrostatic charge pick up. Also, since the input capacitance of a cosmos device is typically 4 pF and the gate impedance is on the order of 10^{12} ohms, the result is a parasitic RC network with a time constant of 4 seconds. Any electrostatic charge can be stored for several seconds, injecting a false logic level into the cosmos device. That could raise havoc with your logic.

If you follow the schematic faithfully, all of the cosmos gates and flip-flops will be used up in fabrication of the keyer, with no surplus devices to cause problems. *Check* and *doublecheck* your wiring!

It's also advisable to provide overvoltage protection and regulation if operation from an unstable supply is anticipated. *Do not* exceed 15 volts, or the cosmos ICs will zener and draw excessive current which may destroy them. I recommend a maximum supply voltage of 12 volts. This should give you plenty of margin for error. Also, be sure to provide a means of protection from accidental polarity reversal of the power supply. Diode CR5 in my supply, fig. 3, provides this protection.

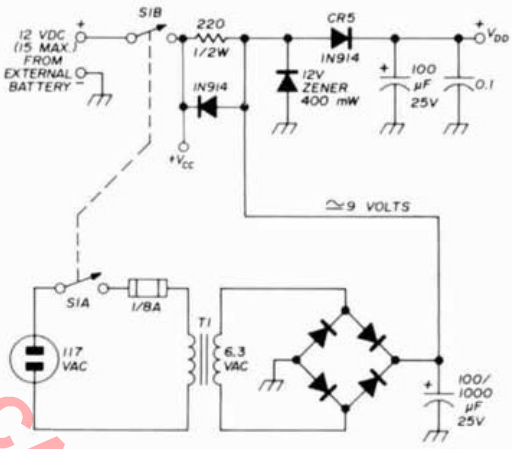
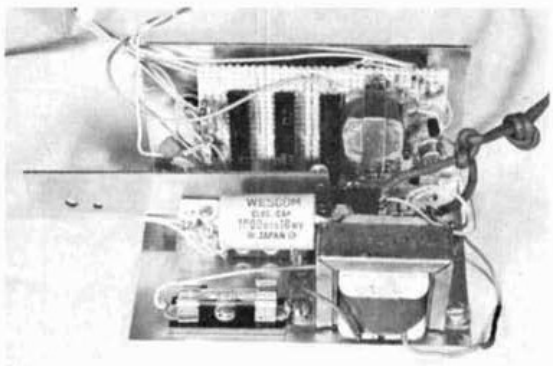


fig. 3. Suggested power supply for cosmos keyer, with inputs for either 117 Vac or low voltage dc. Transformer T1 is a small 6.3 Vac filament transformer.

When soldering cosmos ICs into a circuit, use an iron with a grounded tip. Finally, make sure that your paddle key is clean. Any leakage path to circuit ground that is less than one megohm will falsely trigger the input gates.

The sidetone generator is optional, but can be included if your present rig doesn't have one. The sidetone adds about 3 mA to the key-down current drain.



Main chassis layout. Cosmos circuitry is installed on perforated board, rear; power supply is in foreground.

reference

1. *COSMOS Digital Integrated Cricuits*, RCA Data Book Series, SSD-203A, RCA Semiconductor, 1973.

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