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An Automatic Keyer Using Intergrated Circuits

Here's a very simple integrated circuit keyer that uses very few parts.

This article describes one of many possible applications of integrated circuits to amateur radio. The keyer described is self completing, completely adjustable from less than one word per minute to sixty words per minute, and could be built in a pocket match-box. The complete keyer can be built for less than thirty dollars ($30.00).

Operation

A clock generator consisting of a unijunction transistor and an R-C combination is used to determine the speed of operation. The basic relation of a space equals a dot, and a dash equals three dots was used and is constant regardless of the speed. The clock pulse is connected to the dot flip flop through the logic built into the flip flop package. The output of the dot flip flop drives the dash flip flop. The output of both flip flops are connected to a gate which has an output if either of the inputs go to zero.

The output of the gate in this keyer is used to drive a transistor to control a relay. It is possible to use a transistor only and build in weighting circuits to give individual desired effects; but, the emphasis of this article is on the application of the integrated circuit.

Texas Instruments integrated circuits were available at reasonable prices and were chosen for this application. The SN7302 package (.125 X .250 X .035 inch) contains two flip flops and all of the necessary logic circuits required for proper gating. (38 transistors total) The SN7360 quadruple two input NAND/NOR gate contains 24 transistors total in the same size package. Only one of the four gates in this package is used.

The integrated circuits operate on 3 to 4 volts dc. The minimum voltage which will operate a unijunction transistor properly is 9 Vdc, therefore, a 5.6-volt zener diode is used to drop from 9 Vdc to 3.4 Vdc. The zener diode was chosen over a divider in order to maintain a low power supply impedance for the integrated circuits.

Circuit description

Refer to the schematic diagram. **Fig. 1,** and the logic chart, **Fig. 2.** The capacitor C3 charges up at a rate determined by the speed control R1 and R3. When the voltage across C3 reaches the intrinsic stand-off ratio of Q1 (firing point) C3 is discharged through R4. This provides a positive pulse several milliseconds long with an exponential decay. The flip flops trigger only on the trailing edge of the clock pulse so this signal is passed through C5 and R5 to provide a fast rise and fall pulse.

The terminals marked on the schematic with an asterisk are the dot flip flop. The flip flop operation is as follows: Q. HAS A 2.5 V. output and $\overline{Q}$. (pronounced not Q) is at zero. If K. is positive when a clock pulse is applied to CP. the flip flop switches and Q. and $\overline{Q}$. switch modes. Since J. is connected to +3 volts the following clock pulse reset the flip flop to its original mode. This action represents a dot and space. If the dot key is held down the next clock pulse simply triggers the flip flop again and if the key is released the next pulse resets the flop flop to a space condition and it remains.

The terminals of the SN7302 without an asterisk are used for the dash flip flop.

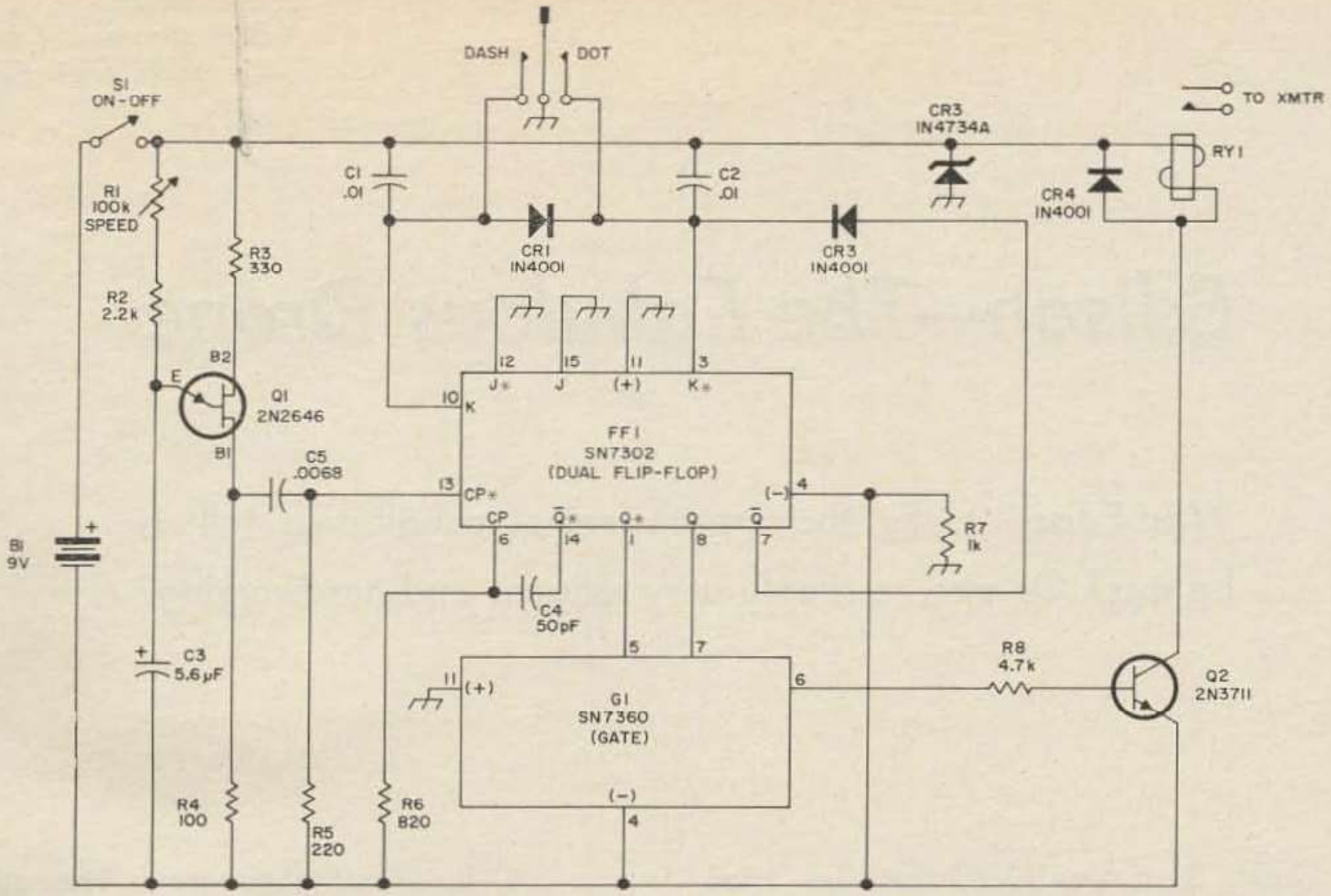

Fig. 1. Schematic of W5FQA's integrated circuit keyer.

The dash operation is as follows: The key is moved to the dash position and a positive voltage is applied to K. through CR1 starting a dot sequence. $\overline{Q}$. goes positive at the start of the dot. This positive signal is differentiated by C4 and R6 providing a fast rise and fall pulse at CP. (The clock pulse input for the dash flip flop.) The input at CP triggers the dash flip flop causing $\overline{Q}$ to go positive since K is positive. The next clock pulse triggers the dot flip flop, but it will not trigger the dash flip flop until $\overline{Q}$. goes positive again which is the following pulse. Then the dash flip flop changes state, but the output of the dot flip flop is still present and will remain for the length of a dot which gives a dash length of 3 dots. If the key is released before a dash is complete a positive voltage is still applied to K. through CR3 which makes the dash self completing.

The operation of the gate SN7360 is as follows: If either and/or both inputs are zero the gate has an output. If both inputs are positive the output is zero.

Information about the integrated circuits used in the keyer is available from Texas Instruments, P.O. Box 5012, Dallas 22, Texas. Request bulletin No. DL-S 657650, July 1965.

Construction

The authors keyer is constructed on a Vero printed board, however, for one who does not have an integrated circuit soldering iron the TI Mech-Pac connectors are ideal. Wiring is not critical and phono wire or #30 to #32 hookup wire is recommended.

The positive 3 volts for the integrated circuits is grounded to prevent floating the common of the key. C1 and C2 shunt any rf to ground. Shielded lead should be used to minimize rf pickup. The battery drain is 30 mA key up and 50 mA key down. A 9 and power obtained from transmitter or receiver B+.
volt zener may be substituted for the battery

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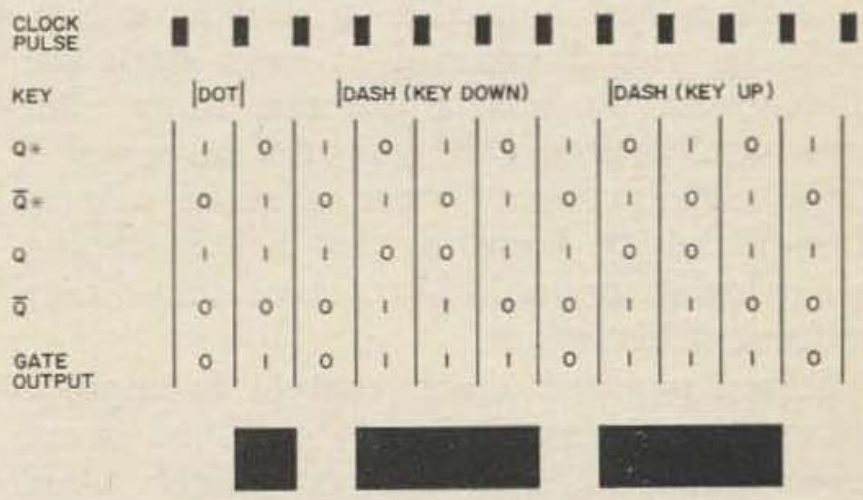

Fig. 2. Logic diagram of the keyer.